L Number	Hits	Search Text	DB	Time stamp
1	1	714/740 and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:06
2	1	714/740 and memory same address same bit same error and (read and write) same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:07
3	1	714/740 and memory same address same bit same error and (read and write) with error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:08
4	0	714/740 and (simulat$ emulat$) and memory same address same bit same error and (read and write) with error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:08
5	21	714/768 and memory same address same bit same error and (read and write) with error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:08
6	4	714/768 and (simulat$ emulat$) and memory same address same bit same error and (read and write) with error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:17
10	3	714/768 and (simulat$ emulat$) and (error near4 (generat$ chang$ creat$)) and memory same address same bit same error and (read and write) with error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:22
11	3	714/768 and (simulat$ emulat$) and (error near4 (generat$ chang$ creat$)) same (read and write) with error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:31
12	1	714/763 and (simulat$ emulat$) and (error near4 (generat$ chang$ creat$)) same (read and write) near4 error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:35
13	0	714/718 and (simulat$ emulat$) and (error near4 (generat$ chang$ creat$)) same (read and write) near4 error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:35

14	1	714/768 and (simulat$ emulat$) and (error near4 (generat$ chang$ creat$)) same (read and write) near4 error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:35
15	0	714/740 and (simulat$ emulat$) and (error near4 (generat$ chang$ creat$)) same (read and write) near4 error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:35
17	0	714/819 and (simulat$ emulat$) and (error near4 (generat$ chang$ creat$)) same (read and write) near4 error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:36
16	1	714/752 and (simulat$ emulat$) and (error near4 (generat$ chang$ creat$)) same (read and write) near4 error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 10:37
19	9	714/$ and (simulat$ emulat$) and (error near4 (generat$3 chang$3 creat$3)) same (read and write) near4 error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:25
20	9	714/$ and (simulat$ emulat$) and (error near3 (generat$3 forc$3 creat$3)) same (read and write) near4 error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:27
21	18	714/$ and (simulat$ emulat$) and (error near (generat$3 forc$3 creat$3)) and (read and write) near4 error and memory same address same bit same error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:30
22	12	714/$ and (simulat$ emulat$) and (error near (generat$3 forc$3 creat$3)) and (read and write) near4 error and memory with address with bit with error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:34
23	4	714/$ and (simulat$ emulat$) and (error near (generat$3 forc$3 creat$3)) same memory with address with bit with error and (read and write) near4 error and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:36
24	0	714/$ and error same (read and write) same memory same (model$3 simulat$3emulat$3) same bit near (first second) same (address location) and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:39

25	0	error same (read and write) same memory same (model$3 simulat$3emulat$3) same bit near (first second) same (address location) and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:39
26	0	error same (read and write) same memory same (model$3 simulat$3emulat$3) same bit near3 (first second) same (address location) and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:40
27	13	error same (read and write) same memory same (model$3 simulat$3emulat$3) same bit same (address location) and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:40
28	1	error same (read and write) same memory near3 (model$3 simulat$3emulat$3) same bit same (address location) and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:41
30	72	error same (read and write) and memory near3 (model$3 simulat$3emulat$3) and error same memory same bit same (address location) and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:41
31	74	error same (read and write) and memory near3 (model$3 simulat$3 emulat$3) and error with (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:46
32	9	error same (read and write) same memory near3 (model$3 simulat$3 emulat$3) and error with (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:47
33	1	error same (read and write) same memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error with (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:48
34	9	error same (read and write) same memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error and error with (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:50
35	0	714/740 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error and error with (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:50

36	0	714/740 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:50
37	1	714/768 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:51
39	0	714/718 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:51
38	1	714/763 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:51
40	0	714/752 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:51
41	0	714/819 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:51
42	1	714/805 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:52
43	0	714/25 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:53
45	2	711/144 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:53
46	0	365/189.01 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:53

47	0	365/189.04 and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 12:53
44	11	714/$ and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 13:02
48	15	711/$ and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 13:03
49	3	703/$ and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 13:07
50	30	memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 16:28
99	3	lsi and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 16:30
102	4	large near scale and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error same (address location) same memory same bit and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 16:33
103	0	(large near scale lsi) and memory near3 (model$3 simulat$3 emulat$3) and (generat$3 forc$3 creat$3 provid$3) near2 error and error same (address location) same memory same bit same revers$3 and (@ad<20000911 @rlad<20000911)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/08/26 16:35

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2 **Analysis of classification performance for Hopfield network with predefined correlated exemplar patterns**
Youngjik Lee; Myung Won Kim; Hyun Kyung Song; Sin Chang Park;
Neural Networks, 1990., 1990 IJCNN International Joint Conference on , 17-21 June 1990
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3 **A convolutional code performance bound for Fritchman single-error state channel models**
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Military Communications Conference, 1995. MILCOM '95, Conference Record, IEEE , Volume: 1 , 5-8 Nov. 1995
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Fault-Tolerant Computing, 1992. FTCS-22. Digest of Papers., Twenty-Second International Symposium on , 8-10 July 1992
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8 **An analysis of the exponential correlation associative memory**
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9 **Associative memory networks, fault-tolerance and coding theory**
Hendrich, N.;
Neural Networks, 1991., IJCNN-91-Seattle International Joint Conference on , Volume: ii , 8-14 July 1991
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10 **Fault tolerant analysis of associative memories**
Huang, Y.-P.; Gustafson, D.;
Neural Networks, 1991. 1991 IEEE International Joint Conference on , 18-21 Nov. 1991
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11 **A neural network based multi-associative memory model**
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Neural Networks, 1990., 1990 IJCNN International Joint Conference on , 17-21 June 1990
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12 **Very low bit video coding algorithm using uncovered region memory**
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13 **An area model for on-chip memories and its application**
Mulder, J.M.; Quach, N.T.; Flynn, M.J.;
Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 2 , Feb. 1991
Pages:98 - 106

[Abstract] [PDF Full-Text (760 KB)] **IEEE JNL**

14 **An associative memory with neural architecture and its VLSI implementation**
Ruckert, U.;
System Sciences, 1991. Proceedings of the Twenty-Fourth Annual Hawaii International Conference on , Volume: i , 8-11 Jan. 1991
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1 An Augmented Content-Addressed Memory Array for Implementation With Large-Scale Integration
William H. Kautz
January 1971 **Journal of the ACM (JACM)**, Volume 18 Issue 1
Full text available: pdf(987.48 KB) Additional Information: full citation, references, citings, index terms

2 A Logic-in-Memory architecture for large-scale-integration technologies
A. M. Peskin
August 1972 **Proceedings of the ACM annual conference - Volume 1**
Full text available: pdf(724.64 KB) Additional Information: full citation, abstract, references, citings, index terms

A computing machine is described which is structured around a distributed logic storage device called the Processing Memory. This machine, the Brookhaven Logic-In-Memory Processor (BLIMP), is meant only as a vehicle for simulating and evaluating its concepts, rather than for eventual fabrication. In particular, it is shown that the architecture used is very well suited to large-scale-integration (LSI) implementation technologies. It was first necessary to redefine the various goals of logic ...

Keywords: Associative memory, Computer architecture, Digital simulation, Logic-in-memory

3 Testing and Debugging Custom Integrated Circuits
Edward H. Frank, Robert F. Sproull
December 1981 **ACM Computing Surveys (CSUR)**, Volume 13 Issue 4
Full text available: pdf(2.25 MB) Additional Information: full citation, references, citings, index terms

4 Dimensionality reduction: On scaling latent semantic indexing for large peer-to-peer systems
Chunqiang Tang, Sandhya Dwarkadas, Zhichen Xu
July 2004 **Proceedings of the 27th annual international conference on Research and development in information retrieval**
Full text available: pdf(208.57 KB) Additional Information: full citation, abstract, references, index terms

The exponential growth of data demands scalable infrastructures capable of indexing and

searching rich content such as text, music, and images. A promising direction is to combine information re-trieval with peer-to-peer technology for scalability, fault-tolerance, and low administration cost. One pioneering work along this di-rection is pSearch [32, 33]. pSearch places documents onto a peer-to- peer overlay network according to semantic vectors produced using Latent Semantic Indexing (LSI). The ...

Keywords: dimensionality reduction, latent semantic indexing, peer-to-peer IR

5 Technical reports
SIGACT News Staff
January 1980 **ACM SIGACT News**, Volume 12 Issue 1
Full text available: pdf(5.28 MB) Additional Information: full citation

6 Experience Using Multiprocessor Systems—A Status Report
Anita K. Jones, Peter Schwarz
June 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 2
Full text available: pdf(4.48 MB) Additional Information: full citation, references, citings, index terms

7 Design of a LISP-based microprocessor
Guy Lewis Steele, Gerald Jay Sussman
November 1980 **Communications of the ACM**, Volume 23 Issue 11
Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, references, citings

We present a design for a class of computers whose "instruction sets" are based on LISP. LISP, like traditional stored-program machine languages and unlike most high-level languages, conceptually stores programs and data in the same way and explicitly allows programs to be manipulated as data, and so is a suitable basis for a stored-program computer architecture. LISP differs from traditional machine languages in that the program/data storage is conceptually an unordered set of ...

Keywords: LISP, SCHEME, VLSI, direct execution, garbage collection, high-level language architectures, integrated circuits, interpreters, large-scale integration, linked lists, list structure, microprocessors, storage management, tail recursion

8 System architectures for computer music
John W. Gordon
June 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 2
Full text available: pdf(4.61 MB) Additional Information: full citation, abstract, references, index terms, review

Computer music is a relatively new field. While a large proportion of the public is aware of computer music in one form or another, there seems to be a need for a better understanding of its capabilities and limitations in terms of synthesis, performance, and recording hardware. This article addresses that need by surveying and discussing the architecture of existing computer music systems. System requirements vary according to what the system will be used for. Common uses for co ...

9 Energy-aware design of embedded memories: A survey of technologies, architectures, and optimization techniques
Luca Benini, Alberto Macii, Massimo Poncino
February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1
Full text available: pdf(288.44 KB) Additional Information: full citation, abstract, references, index terms

Embedded systems are often designed under stringent energy consumption budgets, to limit heat generation and battery size. Since memory systems consume a significant amount of energy to store and to forward data, it is then imperative to balance power consumption and performance in memory system design. Contemporary system design focuses on the trade-off between performance and energy consumption in processing and storage units, as well as in their interconnections. Although memory design is as ...

Keywords: Embedded systems, embedded memories, integration, memories, nonvolatile, system-on-a-chip, volatile

10 The network architecture of the Connection Machine CM-5 (extended abstract)
Charles E. Leiserson, Zahi S. Abuhamdeh, David C. Douglas, Carl R. Feynman, Mahesh N. Ganmukhi, Jeffrey V. Hill, Daniel Hillis, Bradley C. Kuszmaul, Margaret A. St. Pierre, David S. Wells, Monica C. Wong, Shaw-Wen Yang, Robert Zak
June 1992 **Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(2.00 MB) Additional Information: full citation, references, citings, index terms

11 Performance evaluation and improvement of a dynamically microprogrammable computer with low-level parallelism
Shinji Tomita, Kiyoshi Shibayama, Toshiaki Kitamura, Hiroshi Hagiwara
November 1980 **Proceedings of the 13th annual workshop on Microprogramming**
Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, references, citings, index terms

A new microprogrammable computer with low-level parallelism was built and has been utilized as a research vehicle for solving different classes of research-oriented applications such as real-time processings on static/dynamic images, pictures and signals, and emulations of both existing and virtual machines including high (intermediate) level language machines. The design goal of a research-oriented computer, QA-1, was to achieve a high degree of processing power and system flexi ...

12 Hardware for searching very large text databases
Roger Haskin
March 1980 **Proceedings of the fifth workshop on Computer architecture for non-numeric processing**
Full text available: pdf(812.50 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses the problem of searching very large text databases. It is shown that conventional techniques for searching current databases cannot be scaled up to larger ones, and that it is necessary to build hardware to search the database in parallel if reasonable search times are expected. The part of the search process requiring the highest bandwidth is scanning the database to detect instances of search terms. Methods of doing this in hardware that have been mentioned in the lit ...

13 Reducing instruction cache energy consumption using a compiler-based strategy
W. Zhang, J. S. Hu, V. Degalahal, M. Kandemir, N. Vijaykrishnan, M. J. Irwin
March 2004 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 1 Issue 1
Full text available: pdf(1.15 MB) Additional Information: full citation, abstract, references, index terms

Excessive power consumption is widely considered as a major impediment to designing future microprocessors. With the continued scaling down of threshold voltages, the power consumed due to leaky memory cells in on-chip caches will constitute a significant portion of the processor's power budget. This work focuses on reducing the leakage energy consumed in the instruction cache using a compiler-directed approach.We present and analyze two compiler-based strategies termed as conservative and optim ...

Keywords: Leakage power, cache design, compiler optimizations

14 STiNG: a CC-NUMA computer system for the commercial marketplace
Tom Lovett, Russell Clapp
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2
Full text available: pdf(1.30 MB) Additional Information: full citation, abstract, references, citings, index terms

"STiNG" is a Cache Coherent Non-Uniform Memory Access (CC-NUMA) Multiprocessor designed and built by Sequent Computer Systems, Inc. It combines four processor Symmetric Multi-processor (SMP) nodes (called Quads), using a Scalable Coherent Interface (SCI) based coherent interconnect. The Quads are based on the Intel P6 processor and the external bus it defines. In addition to 4 P6 processors, each Quad may contain up to 4 GBytes of system memory, 2 Peripheral Component Interface (PCI) busses for ...

15 Data-Driven and Demand-Driven Computer Architecture
Philip C. Treleaven, David R. Brownbridge, Richard P. Hopkins
January 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 1
Full text available: pdf(4.14 MB) Additional Information: full citation, references, citings, index terms

16 Test generation for LSI: A case study
Magdy S. Abadir, Hassan K. Reghbati
June 1984 **Proceedings of the 21st conference on Design automation**
Full text available: pdf(1.04 MB) Additional Information: full citation, abstract, references, index terms

A new automatic test generation approach for LSI circuits has been presented in the companion papers [1,2]. In this paper we generate tests for a typical LSI circuit using the new approach. The goal of this study is to gain insight into the problems involved in using the test generation procedures. A formal model C for a 1-bit microprocessor slice is defined which has all the main features of commercially available bit slices such as the Am2901. The circuit C is modeled as a network of inte ...

Keywords: Binary decision diagrams, D-propagation, Fault collapsing, Fault detection, Functional modules, Implication, Line justification, Test generation, Test sequences.

17 S-connect: from networks of workstations to supercomputer performance
Andreas G. Nowatzyk, Michael C. Browne, Edmund J. Kelly, Michael Parkin
May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2
Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings, index terms

S-Connect is a new high speed, scalable interconnect system that has been developed to support networks of workstations to efficiently share computing resources. It uses off-the-shelf CMOS technology to directly drive fiber-optic systems at speeds greater than 1 Gbit/sec and can realize bisection bandwidths comparable to high-end MPP systems while being >10x more cost-effective. S-Connect systems do not rely on centralized switches, but rather are composed of adaptive, topology independen ...

18 The evolution of the Sperry Univac 1100 series: a history, analysis, and projection
B. R. Borgerson, M. L. Hanson, P. A. Hartley
January 1978 **Communications of the ACM**, Volume 21 Issue 1
Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, citings, index terms

The 1100 series systems are Sperry Univac's large-scale mainframe computer systems. Beginning with the 1107 in 1962, the 1100 series has progressed through a succession of eight compatible computer models to the latest system, the 1100/80, introduced in 1977. The 1100 series hardware architecture Is based on a 36-bit word, ones complement structure which obtains one operand from storage and one from a high-speed register, or two operands from high-speed registers. The 1100 Operating System ...

Keywords: 1100 computer series, computer architecture, data management systems, end user facilities, executive control software, multiprocessing, multiprogramming, operating system, programming languages

19 Toward a history of (personal) workstations
Gordon Bell
January 1986 **Proceedings of the ACM Conference on The history of personal workstations**

Full text available: pdf(1.48 MB) Additional Information: full citation, abstract, references, citings, index terms

I originally accepted this keynote honor for five reasons: to respond to Alan Perlis' request (he told me I could present anything from a new taxonomy to personal reminiscences); second, to identify the important artifacts that should be preserved in The Computer Museum; third, to posit a framework of the history of workstations that can be written in the next century (we're all too close to create it); fourth, to summarize my own involvement on interactive computing including timesharing a ...

20 Microprogrammed implementation of a single chip microprocessor
Skip Stritter, Nick Tredennick
November 1978 **Proceedings of the 11th annual workshop on Microprogramming**

Full text available: pdf(750.84 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper considers microprogramming as a tool for implementing large scale integration, single-chip microprocessors. Design trade-offs for microprogrammed control are discussed in the context of semiconductor design constraints which limit the size, speed, complexity and pin-out of circuits. Aspects of the control unit of a new generation microprocessor, which has a two level microprogrammed structure, are presented.

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memory and **error** and **address** or **location** and **simulat** or **model** and **bit** and **LSI** or **large scale**

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1 A Logic-in-Memory architecture for large-scale-integration technologies
A. M. Peskin
August 1972 **Proceedings of the ACM annual conference - Volume 1**
Full text available: pdf(724.64 KB) Additional Information: full citation, abstract, references, citings, index terms

A computing machine is described which is structured around a distributed logic storage device called the Processing Memory. This machine, the Brookhaven Logic-In-Memory Processor (BLIMP), is meant only as a vehicle for simulating and evaluating its concepts, rather than for eventual fabrication. In particular, it is shown that the architecture used is very well suited to large-scale-integration (LSI) implementation technologies. It was first necessary to redefine the various goals of logic ...

Keywords: Associative memory, Computer architecture, Digital simulation, Logic-in-memory

2 Testing and Debugging Custom Integrated Circuits
Edward H. Frank, Robert F. Sproull
December 1981 **ACM Computing Surveys (CSUR)**, Volume 13 Issue 4
Full text available: pdf(2.25 MB) Additional Information: full citation, references, citings, index terms

3 Experience Using Multiprocessor Systems—A Status Report
Anita K. Jones, Peter Schwarz
June 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 2
Full text available: pdf(4.48 MB) Additional Information: full citation, references, citings, index terms

4 Dimensionality reduction: On scaling latent semantic indexing for large peer-to-peer systems
Chunqiang Tang, Sandhya Dwarkadas, Zhichen Xu
July 2004 **Proceedings of the 27th annual international conference on Research and development in information retrieval**
Full text available: pdf(208.57 KB) Additional Information: full citation, abstract, references, index terms

The exponential growth of data demands scalable infrastructures capable of indexing and searching rich content such as text, music, and images. A promising direction is to combine information re-trieval with peer-to-peer technology for scalability, fault-tolerance, and low

administration cost. One pioneering work along this di-rection is pSearch [32, 33]. pSearch places documents onto a peer-to- peer overlay network according to semantic vectors produced using Latent Semantic Indexing (LSI). The ...

Keywords: dimensionality reduction, latent semantic indexing, peer-to-peer IR

5 An Augmented Content-Addressed Memory Array for Implementation With Large-Scale Integration
William H. Kautz
January 1971 **Journal of the ACM (JACM)**, Volume 18 Issue 1
Full text available: pdf(987.48 KB) Additional Information: full citation, references, citings, index terms

6 Energy-aware design of embedded memories: A survey of technologies, architectures, and optimization techniques
Luca Benini, Alberto Macii, Massimo Poncino
February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1
Full text available: pdf(288.44 KB) Additional Information: full citation, abstract, references, index terms

Embedded systems are often designed under stringent energy consumption budgets, to limit heat generation and battery size. Since memory systems consume a significant amount of energy to store and to forward data, it is then imperative to balance power consumption and performance in memory system design. Contemporary system design focuses on the trade-off between performance and energy consumption in processing and storage units, as well as in their interconnections. Although memory design is as ...

Keywords: Embedded systems, embedded memories, integration, memories, nonvolatile, system-on-a-chip, volatile

7 Technical reports
SIGACT News Staff
January 1980 **ACM SIGACT News**, Volume 12 Issue 1
Full text available: pdf(5.28 MB) Additional Information: full citation

8 Mos LSI computer aided design system
D. R. Lewallen
January 1969 **Proceedings of the 6th annual conference on Design Automation**
Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, references, citings, index terms

A design system employing computer aided design techniques, a Gerber digital photographic plotter, and an automatic LSI tester has been developed and used in logic design, layout design, mask generation, and testing, of complex MOS Large Scale Integrated circuit arrays. The system employs computer logic simulation for debugging machine logic and generating test tapes, and utilizes abbreviated input data techniques for generating array layout designs and photographic artwork masters. In this ...

9 The network architecture of the Connection Machine CM-5 (extended abstract)
Charles E. Leiserson, Zahi S. Abuhamdeh, David C. Douglas, Carl R. Feynman, Mahesh N. Ganmukhi, Jeffrey V. Hill, Daniel Hillis, Bradley C. Kuszmaul, Margaret A. St. Pierre, David S. Wells, Monica C. Wong, Shaw-Wen Yang, Robert Zak
June 1992 **Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures**

Full text available: pdf(2.00 MB) Additional Information: full citation, references, citings, index terms

10 Design of a LISP-based microprocessor
Guy Lewis Steele, Gerald Jay Sussman
November 1980 **Communications of the ACM**, Volume 23 Issue 11
Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, references, citings

We present a design for a class of computers whose "instruction sets" are based on LISP. LISP, like traditional stored-program machine languages and unlike most high-level languages, conceptually stores programs and data in the same way and explicitly allows programs to be manipulated as data, and so is a suitable basis for a stored-program computer architecture. LISP differs from traditional machine languages in that the program/data storage is conceptually an unordered set of ...

Keywords: LISP, SCHEME, VLSI, direct execution, garbage collection, high-level language architectures, integrated circuits, interpreters, large-scale integration, linked lists, list structure, microprocessors, storage management, tail recursion

11 Computer Communication Networks: Approaches, Objectives, and Performance Considerations
Stephen R. Kimbleton, G. Michael Schneider
September 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 3
Full text available: pdf(3.99 MB) Additional Information: full citation, references, citings, index terms

12 S-connect: from networks of workstations to supercomputer performance
Andreas G. Nowatzyk, Michael C. Browne, Edmund J. Kelly, Michael Parkin
May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2
Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings, index terms

S-Connect is a new high speed, scalable interconnect system that has been developed to support networks of workstations to efficiently share computing resources. It uses off-the-shelf CMOS technology to directly drive fiber-optic systems at speeds greater than 1 Gbit/sec and can realize bisection bandwidths comparable to high-end MPP systems while being >10x more cost-effective. S-Connect systems do not rely on centralized switches, but rather are composed of adaptive, topology independen ...

13 Toward a history of (personal) workstations
Gordon Bell
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14 Designing computer systems with MEMS-based storage
Steven W. Schlosser, John Linwood Griffin, David F. Nagle, Gregory R. Ganger
November 2000 **Proceedings of the ninth international conference on Architectural**

support for programming languages and operating systems, Volume 34 , 28 Issue 5 , 5

Full text available: pdf(439.06 KB) Additional Information: full citation, abstract, references, citings, index terms

For decades the RAM-to-disk memory hierarchy gap has plagued computer architects. An exciting new storage technology based on microelectromechanical systems (MEMS) is poised to fill a large portion of this performance gap, significantly reduce system power consumption, and enable many new applications. This paper explores the system-level implications of integrating MEMS-based storage into the memory hierarchy. Results show that standalone MEMS-based storage reduces I/O stall times by 4-74X over ...

15 The evolution of the DECsystem 10
C. G. Bell, A. Kotok, T. N. Hastings, R. Hill
January 1978 **Communications of the ACM**, Volume 21 Issue 1

Full text available: pdf(1.92 MB) Additional Information: full citation, abstract, references, citings, index terms

The DECsystem 10, also known as the PDP-10, evolved from the PDP-6 (circa 1963) over five generations of implementations to presently include systems covering a price range of five to one. The origin and evolution of the hardware, operating system, and languages are described in terms of technological change, user requirements, and user developments. The PDP-10's contributions to computing technology include: accelerating the transition from batch oriented to time sharing computing systems; ...

Keywords: architecture, computer structures, operating system, timesharing

16 The evolution of the Sperry Univac 1100 series: a history, analysis, and projection
B. R. Borgerson, M. L. Hanson, P. A. Hartley
January 1978 **Communications of the ACM**, Volume 21 Issue 1

Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, citings, index terms

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Keywords: 1100 computer series, computer architecture, data management systems, end user facilities, executive control software, multiprocessing, multiprogramming, operating system, programming languages

17 Designing computer systems with MEMS-based storage
Steven W. Schlosser, John Linwood Griffin, David F. Nagle, Gregory R. Ganger
November 2000 **ACM SIGPLAN Notices**, Volume 35 Issue 11

Full text available: pdf(439.06 KB) Additional Information: full citation, abstract, references, index terms

For decades the RAM-to-disk memory hierarchy gap has plagued computer architects. An exciting new storage technology based on microelectromechanical systems (MEMS) is poised to fill a large portion of this performance gap, significantly reduce system power consumption, and enable many new applications. This paper explores the system-level implications of integrating MEMS-based storage into the memory hierarchy. Results show that standalone MEMS-based storage reduces I/O stall times by 4--74X ove ...

18 A simulation approach to the reliability analysis of main storage systems
S. K. Kwon, H. E. Harvey
March 1979 **Proceedings of the twelfth annual simulation symposium**

Full text available: pdf(846.51 KB) Additional Information: full citation, abstract, references, index terms

The Monte Carlo technique has been employed in studying the behavior of main storage systems with single error correction in terms of uncorrectable error rate and storage card replacement rate under various maintenance conditions in the field. It has been demonstrated that such a simulation approach is very powerful and practical when the component hazard rates vary with time, and that the results of this analysis can be used in determining an optimum maintenance strategy that minimizes the ...

19 Performance evaluation and improvement of a dynamically microprogrammable computer with low-level parallelism
Shinji Tomita, Kiyoshi Shibayama, Toshiaki Kitamura, Hiroshi Hagiwara
November 1980 **Proceedings of the 13th annual workshop on Microprogramming**

Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, references, citings, index terms

A new microprogrammable computer with low-level parallelism was built and has been utilized as a research vehicle for solving different classes of research-oriented applications such as real-time processings on static/dynamic images, pictures and signals, and emulations of both existing and virtual machines including high (intermediate) level language machines. The design goal of a research-oriented computer, QA-1, was to achieve a high degree of processing power and system flexi ...

20 Hardware for searching very large text databases
Roger Haskin
March 1980 **Proceedings of the fifth workshop on Computer architecture for non-numeric processing**

Full text available: pdf(812.50 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses the problem of searching very large text databases. It is shown that conventional techniques for searching current databases cannot be scaled up to larger ones, and that it is necessary to build hardware to search the database in parallel if reasonable search times are expected. The part of the search process requiring the highest bandwidth is scanning the database to detect instances of search terms. Methods of doing this in hardware that have been mentioned in the lit ...

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